WHAT IS CLAIMED IS:

1. An apparatus comprising:

an electrically powered physical layer interface to interface between a bus and a network, the physical layer interface having a high power state and a low power state; and

a power management system configured to transition the physical layer interface to the low power state when a signal is detected on the bus.

2. The apparatus of claim 1, wherein the bus is a PCI bus.

3. The apparatus of claim 1, wherein the bus is a PCI-X bus.

4. The apparatus of claim 2, wherein the signal is a PCI reset signal assertion.

5. The apparatus of claim 3, wherein the signal is a PCI reset signal assertion.

6. The apparatus of claim 1, wherein the low power state is when the physical layer interface is powered off.

7. The apparatus of claim 1, wherein the low power state is when the physical layer interface draws no more than a predetermined amount of current.

8. The apparatus of claim 4, wherein the physical layer interface has a plurality of different low power states and the power management system is configured to transition the physical layer interface to one of the plurality of low power states when a PCI reset signal assertion is detected.

9. The apparatus of claim 8, wherein the one of the plurality of low power states is when the physical layer interface is powered off.

10. The apparatus of claim 4, wherein the power management system is hard wired into a Gigabit Ethernet device.

11. The apparatus of claim 10, wherein the low power state is when the physical layer interface is transmitting or receiving data at no greater than 100 megabits per second.

12. A system comprising:

a power supply;

a bus electrically connected to the power supply;

a central processing unit in communication with the bus; and

a communications device in communication with bus, the communications device comprising:

an electrically powered physical layer interface having a high power state and a low power state; and

a power management system configured to transition the physical layer interface to the low power state when a signal is detected on the bus.

13. The system of claim 12, wherein the bus is a PCI bus and the signal is a PCI reset signal assertion.

14. The system of claim 12, wherein the bus is a PCI-X bus and the signal is a PCI reset signal assertion.

15. The system of claim 13, wherein the physical layer interface has a plurality of different low power states and the power management system is configured to transition the physical layer interface to one of the plurality of low power states when a PCI reset signal assertion is detected.

16. The system of claim 15, wherein the physical layer interface has two low power states, an off power state and a low power state.

17. The system of claim 16, wherein the communications device includes a register having at least a one-bit field, and the system further comprises:

a storage device;

an operating system stored on the storage device and configured to write data to the field in the register if wake up of the communications device is enabled or disabled; and

wherein the power management system is configured to transition the physical layer interface to the off power state when a PCI reset signal assertion is detected if the data in the register indicates that wake up is disabled when a PCI reset signal assertion is detected, and transition the physical layer interface to the low power state when a PCI reset signal assertion is detected if the data in the register indicates that wake up is enabled when the PCI reset signal assertion is detected.

18. The system of claim 17, wherein the communications device is a Gigabit Ethernet device.

19. The system of claim 18, wherein the low power state of the physical layer interface is when the physical layer interface transmits or receives data at less than or equal to 100 megabits per second.

20. The system of claim 12, wherein the communication device is a wireless local area network controller.

21. The system of claim 18 wherein the power management system is hard wired into the Gigabit Ethernet device.

22. A method comprising:

monitoring a bus by a device with an electrically powered physical layer interface having a high power state and at least one low power state within a networked computer system having an operating system; and

changing the power state of a physical layer interface to a low power state when a signal is detected on the bus.

23. The method of claim 22 wherein the device is a Gigabit Ethernet device.

24. The method of claim 23, further comprising:

providing a register within the device;

writing data to the register by the operating system to indicate whether wake up of the device is enabled or disabled;

changing the power state of the physical layer interface to an first low power state when the signal is detected by the device if the data in the register indicates that wake up is disabled at the time the signal is detected; and

changing the power state of the physical layer interface to a second low power state when the signal is detected by the device if the data in the register indicates that wake up is enabled at the time the signal is detected.

25. The method of claim 24 wherein the device comprises a Gigabit Ethernet device.

26. The method of claim 25 wherein the first low power state is when the physical layer interface is not enabled to transmit data to or receive data from the network.

27. The method of claim 26 wherein the second low power state is when the physical layer interface is configured to transmit data to or receive data from the network up to 100 megabits per second.

28. The method of claim 27 wherein the bus is a PCI bus and the signal is a PCI reset assertion.

29. The method of claim 27 wherein the bus is a PCI-X bus and the signal is a PCI reset assertion.

30. A computer program product residing on a computer readable medium for powering down a physical layer interface, comprising instructions for causing a device to:

monitor a bus for assertion of a signal on the bus; and

change the power state of the physical layer interface to a low power state when the signal is detected on the bus.

31. The computer program product of claim 30 wherein the device is a Gigabit Ethernet device.

32. The computer program product of claim 30, further comprising instructions to:

write data to a register by the operating system to indicate whether wake up of the device is enabled or disabled;

change the power state of the physical layer interface to an first low power state when the signal is detected by the device if the data in the register indicates that wake up is disabled at the time the signal is detected or to a second low

power state when the signal is detected by the device if the data in the register indicates that wake up is enabled at the time the signal is detected.